Si4133G-X2

DUAL-BAND RF SYNTHESIZER WITH INTEGRATED VCOS FOR GSM AND GPRS WIRELESS COMMUNICATIONS

Features

- Dual-Band RF Synthesizers
  - RF1: 900 MHz to 1.8 GHz
  - RF2: 750 MHz to 1.5 GHz
- IF Synthesizer
  - 1070.4, 1080, and 1089.6 MHz
- Integrated VCOs, Loop Filters, Varactors, and Resonators
- Minimal External Components Required
- Optimized for Use with Hitachi Bright2+ Transceiver
- Settling Time < 150 µs
- Low Phase Noise
- Programmable Power Down Modes
- 1 µA Standby Current
- 18 mA Typical Supply Current
- 2.7 V to 3.6 V Operation
- Packages: 24-Pin TSSOP and 28-Pin MLP

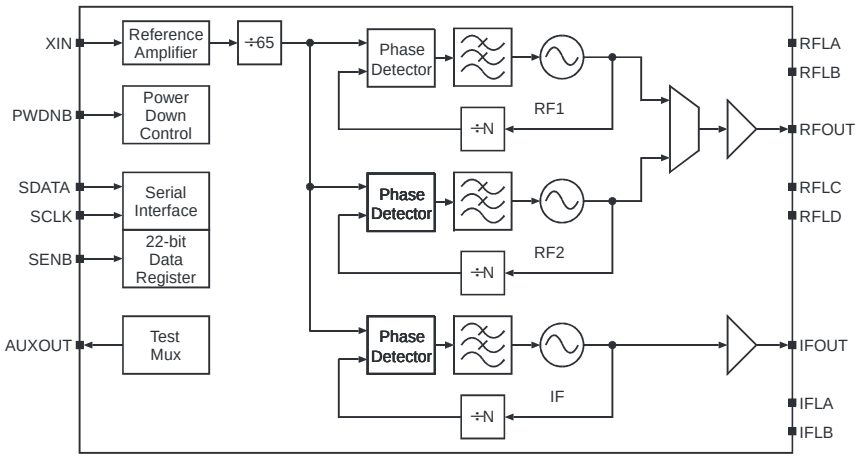
Applications

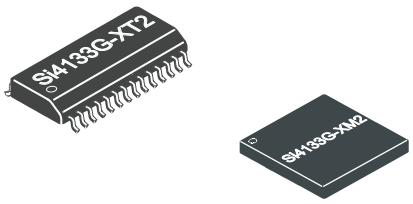
- GSM900, DCS1800, and PCS1900 Cellular Telephones
- GPRS Data Terminals
- HSCSD Data Terminals

Description

The Si4133G-X2 is a monolithic integrated circuit that performs both IF and dual-band RF synthesis for GSM and GPRS wireless communications applications. The Si4133G-X2 includes three VCOs, loop filters, reference and VCO dividers, and phase detectors. Divider and power down settings are programmable through a three-wire serial interface.

Functional Block Diagram



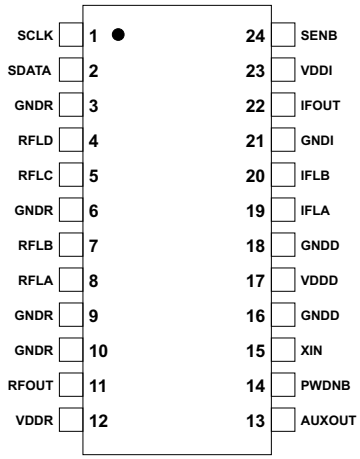


Ordering Information

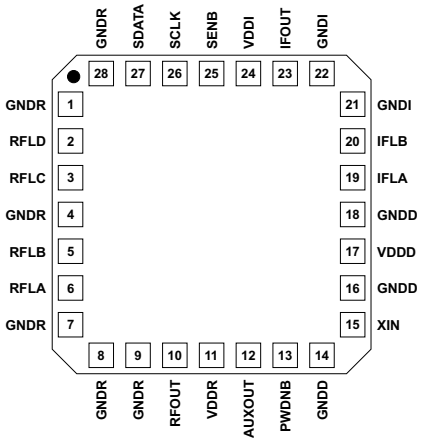
See page 27.

Pin Assignments

Si4133G-XT2



Si4133G-XM2



Patents pending

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Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–20	25	85	°C
Supply Voltage	V_{DD}		2.7	3.0	3.6	V
Supply Voltages Difference	V_Δ	$(V_{DDR} – V_{DDD})$, $(V_{DDI} – V_{DDD})$	–0.3	—	0.3	V

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at 3.0 V and an operating temperature of 25°C unless otherwise stated.

Table 2. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 4.0	V
Input Current[3]	I_{IN}	±10	mA
Input Voltage[3]	V_{IN}	-0.3 to V_{DD}+0.3	V
Storage Temperature Range	T_{STG}	–55 to 150	^oC

Notes:

1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. **This device is a high performance RF integrated circuit with an ESD rating of < 2 kV. Handling and assembly of this device should only be done at ESD-protected workstations.**
3. For signals SCLK, SDATA, SENB, PWDNB and XIN.

Table 3. DC Characteristics
(V_{DD} = 2.7 to 3.6 V, T_A = –20 to 85°C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Total Supply Current[1]		RF1 and IF operating	—	18	31	mA
RF1 Mode Supply Current[1]			—	13	17	mA
RF2 Mode Supply Current[1]			—	12	17	mA
IF Mode Supply Current[1]			—	10	14	mA
Standby Current		PWDNB = 0, XPDM = 0	—	1	—	µA
High Level Input Voltage[2]	V_{IH}		0.7 V_{DD}	—	—	V
Low Level Input Voltage[2]	V_{IL}		—	—	0.3 V_{DD}	V
High Level Input Current[2]	I_{IH}	V_{IH} = 3.6 V, V_{DD} = 3.6 V	–10	—	10	µA
Low Level Input Current[2]	I_{IL}	V_{IL} = 0 V, V_{DD}= 3.6 V	–10	—	10	µA
High Level Output Voltage[3]	V_{OH}	I_{OH} = –500 µA	V_{DD}–0.4	—	—	V
Low Level Output Voltage[3]	V_{OL}	I_{OH} = 500 µA	—	—	0.4	V

Notes:
1. RF1 = 1.55 GHz, RF2 = 1.2 GHz, IF = 1080 MHz, RFPWR = 1
2. For signals SCLK, SDATA, SENB, and PWDNB.
3. For signal AUXOUT.

Table 4. Serial Interface Timing
(V_{DD} = 2.7 to 3.6 V, T_A = –20 to 85°C)

Parameter[1]	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Cycle Time	t_{clk}	Figure 1	40	—	—	ns
SCLK Rise Time	t_r	Figure 1	—	—	50	ns
SCLK Fall Time	t_f	Figure 1	—	—	50	ns
SCLK High Time	t_h	Figure 1	10	—	—	ns
SCLK Low Time	t_l	Figure 1	10	—	—	ns
SDATA Setup Time to SCLK↑[2]	t_{su}	Figure 2	5	—	—	ns
SDATA Hold Time from SCLK↑[2]	t_{hold}	Figure 2	0	—	—	ns
SENB↓ to SCLK↑ Delay Time[2]	t_{en1}	Figure 2	10	—	—	ns
SCLK↑ to SENB↑ Delay Time[2]	t_{en2}	Figure 2	12	—	—	ns
SENB↑ to SCLK↑ Delay Time[2]	t_{en3}	Figure 2	12	—	—	ns
SENB Pulse Width	t_w	Figure 2	10	—	—	ns

Notes:
1. All timing is referenced to the 50% level of the waveform, unless otherwise noted.
2. Timing is not referenced to 50% level of waveform. See Figure 2.

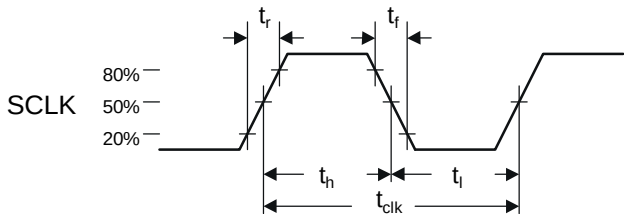


Figure 1. SCLK Timing Diagram

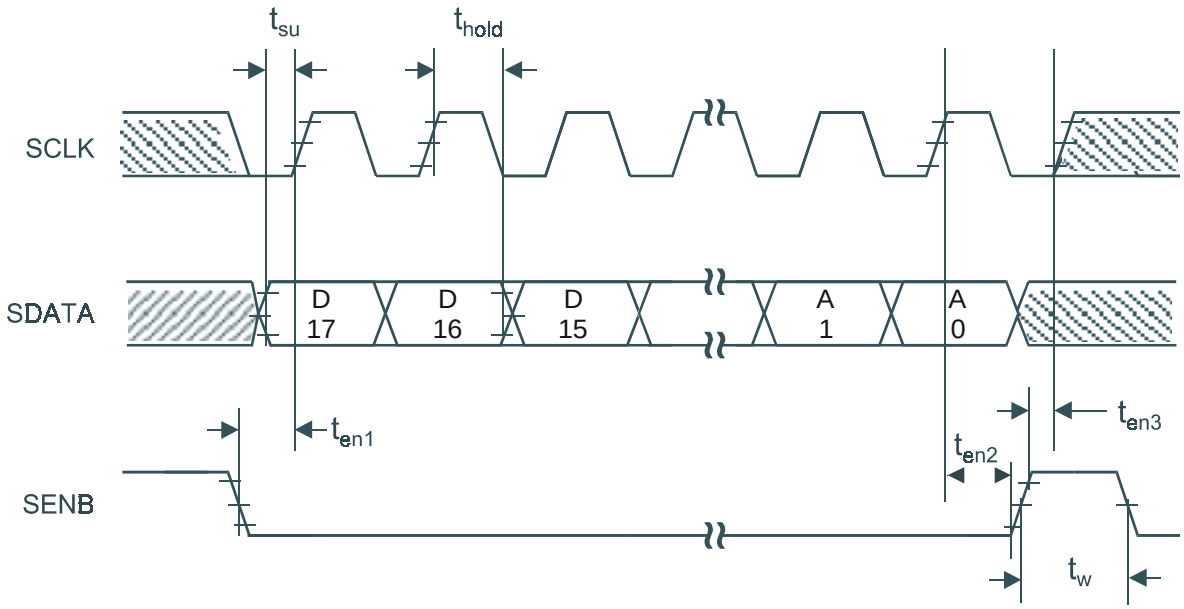


Figure 2. Serial Interface Timing Diagram

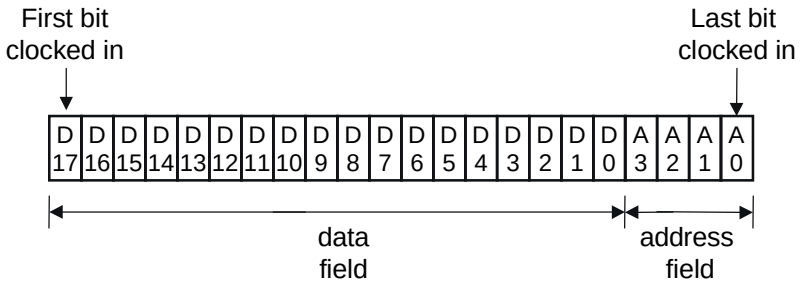


Figure 3. Serial Word Format

Table 5. RF and IF Synthesizer Characteristics
(V_{DD} = 2.7 to 3.6 V, T_A = –20 to 85°C)

Parameter[1]	Symbol	Test Condition	Min	Typ	Max	Unit
XIN Input Frequency	f_{REF}		—	13	—	MHz
Reference Amplifier Sensitivity	V_{REF}		0.5	—	V_{DD} +0.3	V_{P-P}
Internal Phase Detector Frequency	f_ϕ	$f_\phi = f_{REF}/R$		200		KHz
RF1 VCO Center Frequency Range	f_{CEN}		947	—	1720	MHz
RF2 VCO Center Frequency Range	f_{CEN}		789	—	1429	MHz
IFOUT Center Frequency	f_{CEN}		—	1080	—	MHz
Tuning Range from f_{CEN}		Note: L_{EXT} ±10%	–5	—	+5	%
RF1 VCO Pushing		Open loop	—	0.5	—	MHz/V
RF2 VCO Pushing			—	0.4	—	MHz/V
IF VCO Pushing			—	0.3	—	MHz/V
RF1 VCO Pulling		VSWR = 2:1, all phases, open loop	—	0.4	—	MHz_{p-p}
RF2 VCO Pulling			—	0.1	—	MHz_{p-p}
IF VCO Pulling			—	0.1	—	MHz_{p-p}
RF1 Phase Noise		1 MHz offset	—	–132	—	dBc/Hz
		3 MHz offset	—	–142	—	dBc/Hz
RF2 Phase Noise		1 MHz offset	—	–134	—	dBc/Hz
		3 MHz offset	—	–144	—	dBc/Hz
IF Phase Noise		100 kHz offset	—	–117	—	dBc/Hz
RF1 Integrated Phase Error		100 Hz to 100 kHz	—	0.9	—	deg rms
RF1 Harmonic Suppression		Second Harmonic	—	–26		dBc
RF2 Harmonic Suppression			—	–26		dBc
IF Harmonic Suppression			—	–26		dBc
RFOUT Power Level		Z_L = 50 Ω	–7	–2	1	dBm
IFOUT Power Level		Z_L = 50 Ω	–10	–6	–3	dBm

Notes:
1. RF1 = 1.55 GHz, RF2 = 1.4 GHz, IF = 1080 MHz., RFPWR=0 for all parameters unless otherwise noted.
2. From power up request (PWDNB↑ or SENB↑ during a write of 1 to bits PDAB, PDIB, and PDRB in register 2) to RF and IF synthesizers ready (settled to within 0.1 ppm frequency error). Typical settling time to 5 degrees phase error is 120 µs.
3. From power down request (PWDNB↓, or SENB↑ during a write of 0 to bits PDAB, PDIB, and PDRB in register 2) to supply current equal to I_{PWDN}.

Table 5. RF and IF Synthesizer Characteristics (Continued)
(V_{DD} = 2.7 to 3.6 V, T_A = –20 to 85°C)

Parameter[1]	Symbol	Test Condition	Min	Typ	Max	Unit
RF1 Reference Spurs		Offset = 200 kHz	—	–70	—	dBc
		Offset = 400 kHz	—	–75	—	dBc
		Offset = 600 kHz	—	–80	—	dBc
RF2 Reference Spurs		Offset = 200 kHz	—	–75	—	dBc
		Offset = 400 kHz	—	–80	—	dBc
		Offset = 600 kHz	—	–80	—	dBc
Power Up Request to Synthesizer Ready Time, RF1, RF2, IF[2]	t_{pup}	Figures 4, 5	—	140	—	µs
Power Down Request to Synthesizer Off Time[3]	t_{pdn}	Figures 4, 5	—	—	100	ns

Notes:
1. RF1 = 1.55 GHz, RF2 = 1.4 GHz, IF = 1080 MHz., RFPWR=0 for all parameters unless otherwise noted.
2. From power up request (PWDNB↑ or SENB↑ during a write of 1 to bits PDAB, PDIB, and PDRB in register 2) to RF and IF synthesizers ready (settled to within 0.1 ppm frequency error). Typical settling time to 5 degrees phase error is 120 µs.
3. From power down request (PWDNB↓, or SENB↑ during a write of 0 to bits PDAB, PDIB, and PDRB in register 2) to supply current equal to I_{PWDN}.

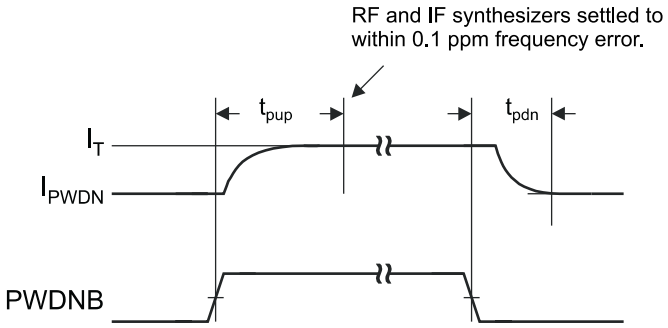


Figure 4. Hardware Power Management Timing Diagram

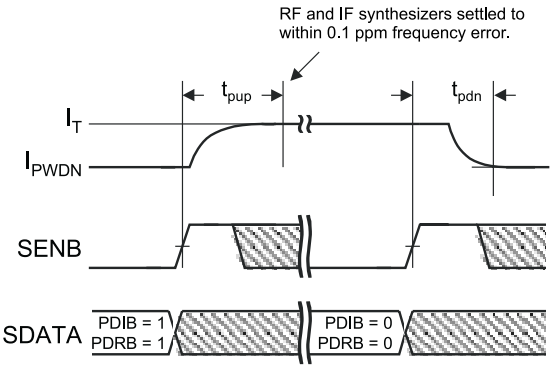


Figure 5. Software Power Management Timing Diagram

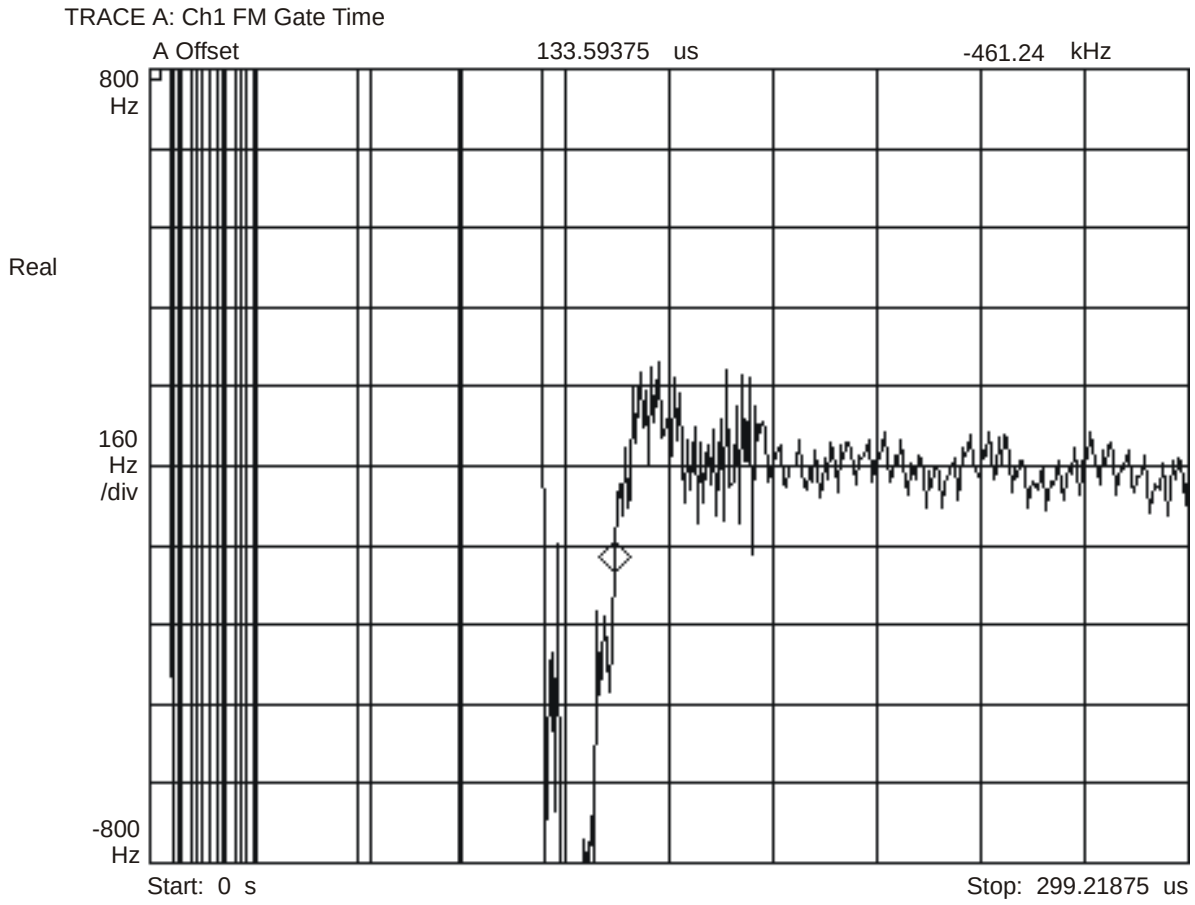


Figure 6. Typical Transient Response RF1 at 1.6 GHz with 200 kHz Phase Detector Update Frequency

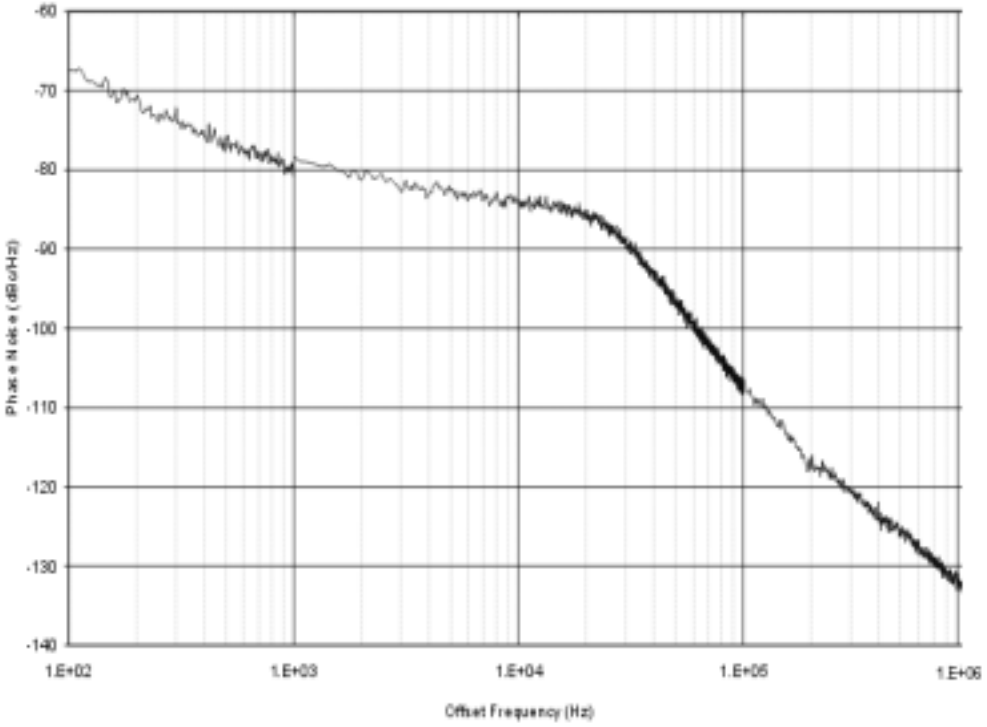


Figure 7. Typical RF1 Phase Noise at 1.6 GHz with 200 kHz Phase Detector Update Frequency

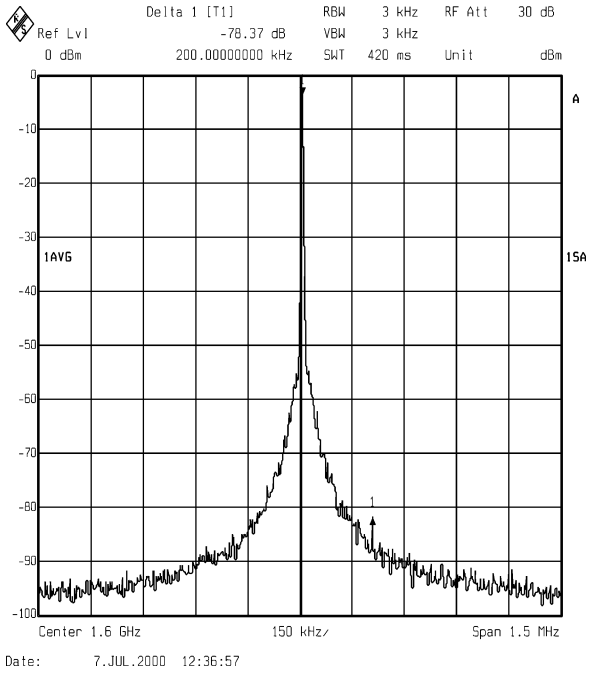


Figure 8. Typical RF1 Spurious Response at 1.6 GHz with 200 kHz Phase Detector Update Frequency

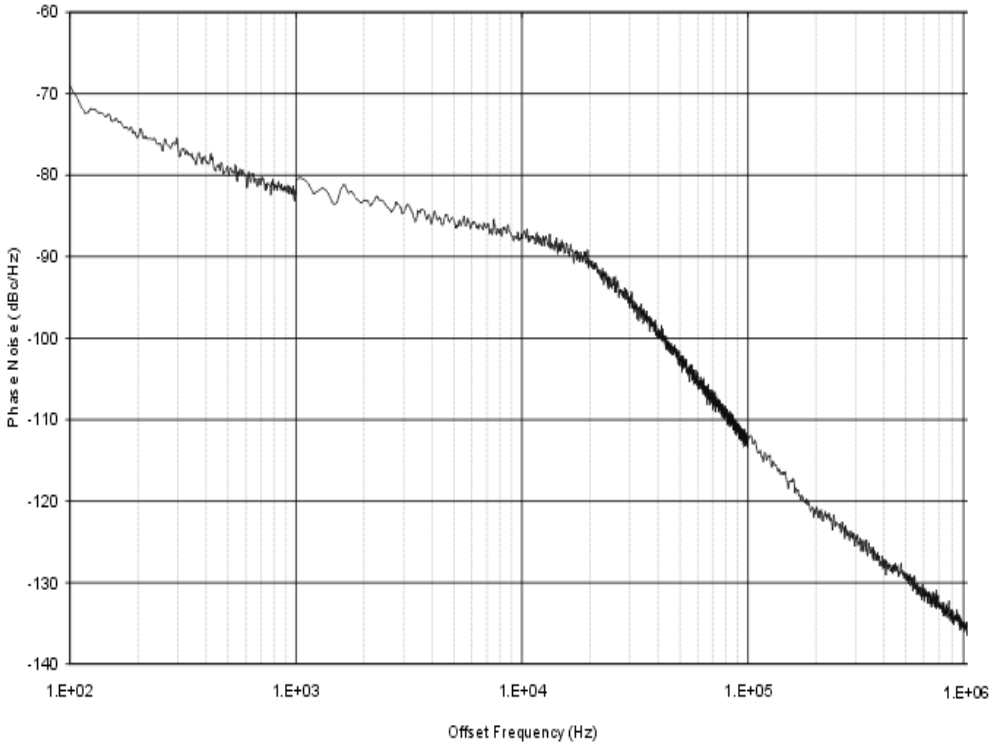


Figure 9. Typical RF2 Phase Noise at 1.2 GHz with 200 kHz Phase Detector Update Frequency

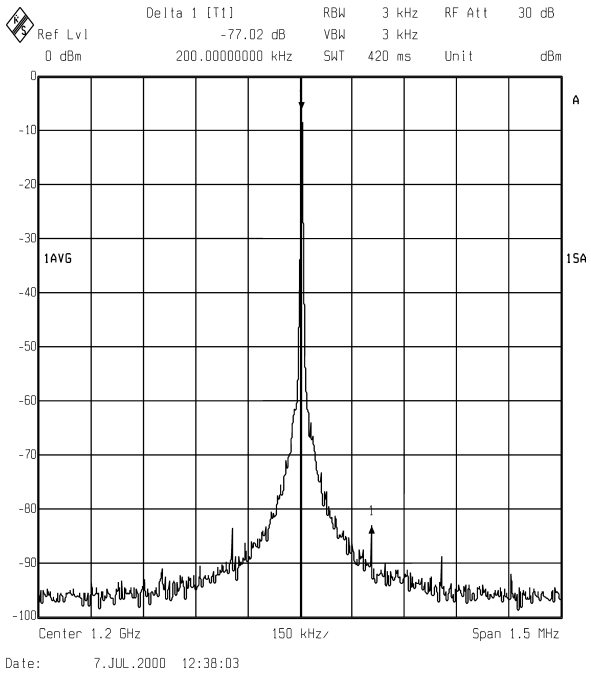


Figure 10. Typical RF2 Spurious Response at 1.2 GHz with 200 kHz Phase Detector Update Frequency

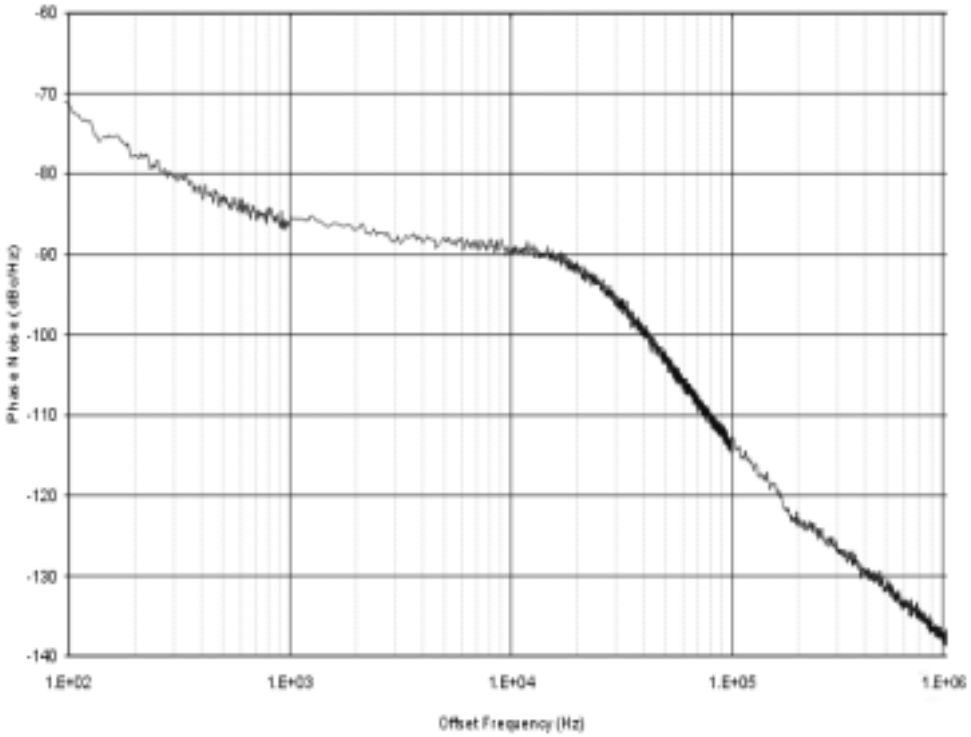


Figure 11. Typical IF Phase Noise at 1080 MHz with 200 kHz Phase Detector Update Frequency

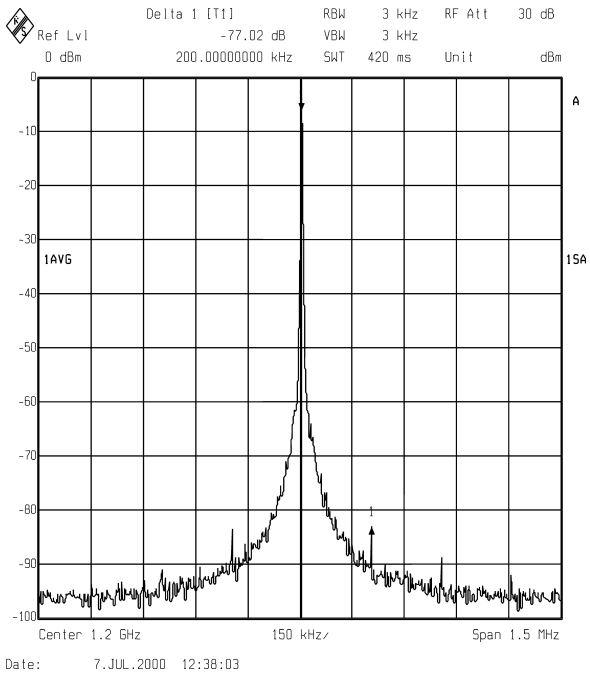


Figure 12. IF Spurious Response at 1080 MHz with 200 kHz Phase Detector Update Frequency

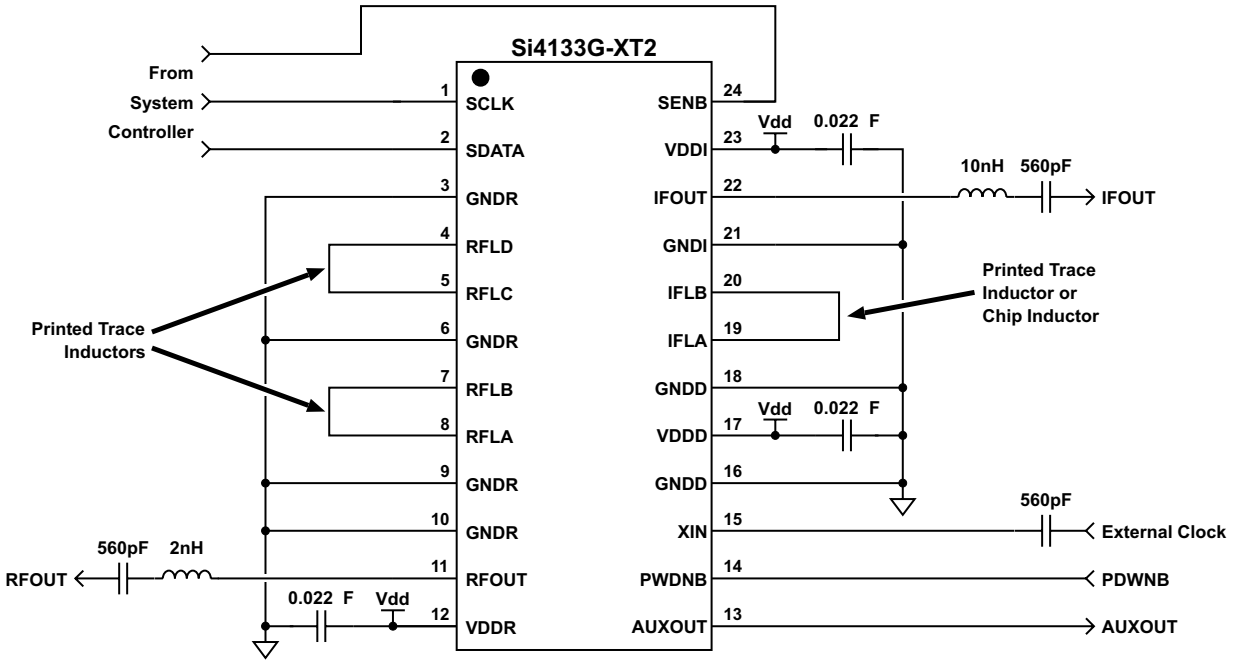


Figure 13. Typical Application Circuit: Si4133G-XT2

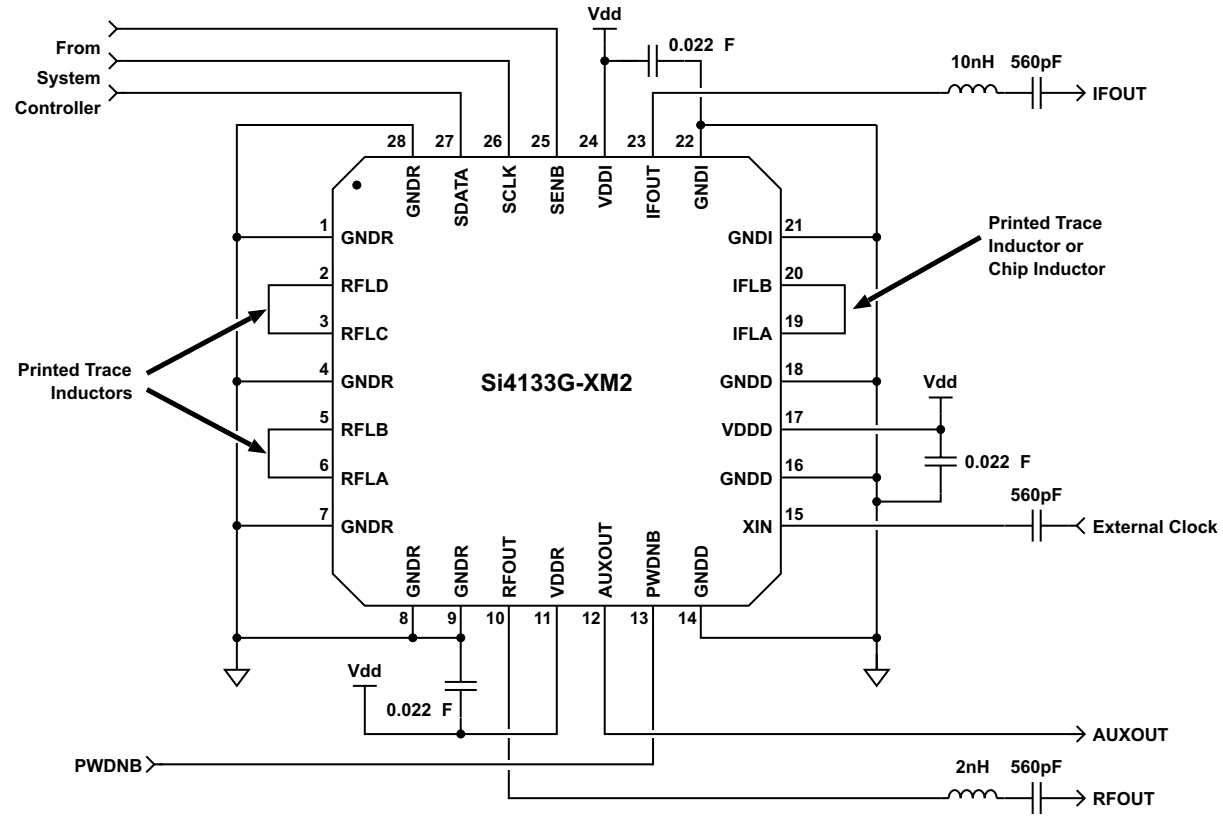


Figure 14. Typical Application Circuit: Si4133G-XM2

Functional Description

The Si4133G-X2 is a monolithic integrated circuit that performs IF and dual-band RF synthesis for many wireless applications such as GSM900, DCS1800, and PCS1900. Its fast transient response also makes the Si4133G-X2 especially well suited to GPRS and HSCSD multislot applications where channel switching and settling times are critical. This integrated circuit (IC), with a minimum number of external components, is all that is necessary to implement the frequency synthesis function.

The Si4133G-X2 has three complete phase-locked loops (PLLs) with integrated voltage-controlled oscillators (VCOs). The low phase noise of the VCOs makes the Si4133G-X2 suitable for use in demanding cellular applications. Also integrated are phase detectors, loop filters, and reference dividers. The IC is programmed through a three-wire serial interface.

One PLL is provided for IF synthesis, and two PLLs are provided for dual-band RF synthesis. One RF VCO is optimized to have its center frequency set between 947 MHz and 1720 MHz, while the second RF VCO is optimized to have its center frequency set between 789 MHz and 1429 MHz. Each RF PLL can adjust its output frequency by ±5% relative to its VCO's center frequency. The IF VCO is optimized to have its center frequency set to 1080 MHz. Three settings are provided for IF output frequencies of 1070.4 MHz, 1080 MHz and 1089.6 MHz.

The center frequency of each of the three VCOs is set by connection of an external inductance. Inaccuracies in the value of the inductance are compensated for by the Si4133G-X2's proprietary self-tuning algorithm. This algorithm is initiated each time the PLL is powered-up (by either the PWDNB pin or by software) and/or each time a new output frequency is programmed.

The two RF PLLs share a common output pin, so only one PLL is active at a given time. Because the two VCOs can be set to have widely separated center frequencies, the RF output can be programmed to service different frequency bands, thus making the Si4133G-X2 ideal for use in dual-band cellular handsets.

The unique PLL architecture used in the Si4133G-X2 produces a transient response that is superior in speed to fractional-N architectures without suffering the high phase noise or spurious modulation effects often associated with those designs.

Serial Interface

The Si4133G-X2 is programmed serially with 22-bit words comprised of 18-bit data fields and 4-bit address fields. Figure 3 on page 7 shows the format of the serial interface. A timing diagram for the serial word is shown in Figure 2 on page 7.

When the serial interface is enabled (i.e., when SENB is low) data and address bits on the SDATA pin are clocked into an internal shift register on the rising edge of SCLK. Data in the shift register is then transferred on the rising edge of SENB into the internal data register addressed in the address field. The serial word is disabled when SENB is high.

Table 9 on page 20 summarizes the data register functions and addresses. It is not necessary (although it is permissible) to clock into the internal shift register any leading bits that are "don't cares".

Setting the VCO Center Frequencies

The PLLs can adjust the IF and RF output frequencies ±5% with respect to their VCO center frequencies. Each center frequency is established by the value of an external inductance connected to the respective VCO. Manufacturing tolerances of ±10% for the external inductances are acceptable. The Si4133G-X2 will compensate for inaccuracies in each inductance by executing a self-tuning algorithm following power-up or following a change in the programmed output frequency.

Because the total tank inductance is in the low nH range, the inductance of the package needs to be considered in determining the correct external inductance. The total inductance (L_{TOT}) presented to each VCO is the sum of the external inductance (L_{EXT}) and the package inductance (L_{PKG}). Each VCO has a nominal capacitance (C_{NOM}) in parallel with the total inductance, and the center frequency is as follows:

$$F_{CEN} = \frac{1}{2\pi\sqrt{L_{TOT} \cdot C_{NOM}}}$$

or

$$F_{CEN} = \frac{1}{2\pi\sqrt{(L_{PKG} + L_{EXT}) \cdot C_{NOM}}}$$

Tables 6 and 7 summarize these characteristics for each VCO.

Table 6. Si4133G-XT2 VCO Characteristics

VCO	f_{CEN} Range (MHz)		Cnom (pF)	Lpkg (nH)	Lext Range (nH)	
	Min	Max			Min	Max
RF1	947	1720	4.3	2.0	0.0	4.6
RF2	789	1429	4.8	2.3	0.3	6.2
IF	1080		6.5	2.1	1.2	

Table 7. Si4133G-XM2 VCO Characteristics

VCO	f_{CEN} Range (MHz)		Cnom (pF)	Lpkg (nH)	Lext Range (nH)	
	Min	Max			Min	Max
RF1	947	1720	4.3	1.5	0.5	5.1
RF2	789	1429	4.8	1.5	1.1	7.0
IF	1080		6.5	1.6	1.7	

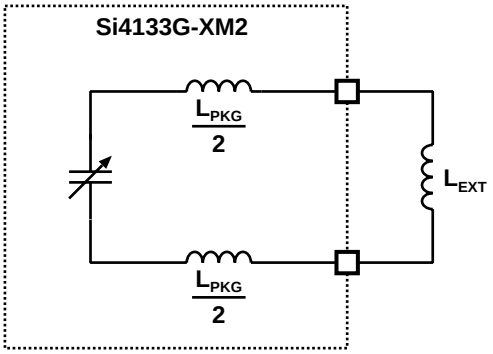


Figure 15. External Inductance Connection

As a design example, suppose it is desired to synthesize frequencies in a 25 MHz band between 1120 MHz and 1145 MHz. The center frequency should be defined as midway between the two extremes, or 1132.5 MHz. The PLL will be able to adjust the VCO output frequency ±5% of the center frequency, or ±56.6 MHz of 1132.5 MHz (i.e., from approximately 1076 MHz to 1189 MHz, more than enough for this example). The RF2 VCO has a C_{NOM} of 4.8 pF, and a 4.1 nH inductance (correct to two digits) in parallel with this capacitance will yield the desired center frequency. An external inductance of 1.8 nH should be connected between RFLC and RFLD as shown in Figure 15. This, in addition to 2.3 nH of package inductance, will present the correct total inductance to the VCO. In manufacturing, the external inductance can vary ±10% of its nominal value and the Si4133G-X2 will correct for the variation with the self-tuning algorithm.

In most cases the requisite value of the external inductance is small enough to allow a PC board trace to be utilized. During initial board layout, a length of trace approximating the desired inductance can be used. For more information, please refer to Application Note 31.

Self-Tuning Algorithm

The self-tuning algorithm is initiated immediately following power-up of a PLL or, if the PLL is already powered, following a change in its programmed output frequency. This algorithm attempts to tune the VCO so that its free-running frequency is near the desired output frequency. In so doing, the algorithm will compensate for manufacturing tolerance errors in the value of the external inductance connected to the VCO. It will also reduce the frequency error for which the PLL must correct to get the precise desired output frequency. The self-tuning algorithm will leave the VCO oscillating at a frequency in error by somewhat less than 1% of the desired output frequency.

After self-tuning, the PLL controls the VCO oscillation frequency. The PLL will complete frequency locking, eliminating any remaining frequency error. Thereafter, it will maintain frequency-lock, compensating for effects caused by temperature and supply voltage variations.

The Si4133G-X2's self-tuning algorithm will compensate for component value errors at any temperature within the specified temperature range. However, the ability of the PLL to compensate for drift in component values that occur AFTER self-tuning is limited. For external inductances with temperature coefficients around ±150 ppm/^{o}C, the PLL will be able to maintain lock for changes in temperature of approximately ±30^{o}C.

Applications where the PLL is regularly powered down or switched between channels minimize or eliminate the potential effects of temperature drift because the VCO is re-tuned when it is powered up or when a new frequency is programmed. In applications where the ambient temperature can drift substantially after self-tuning, it may be necessary to monitor the LDETB (lock-detect bar) signal on the AUXOUT pin to determine the locking state of the PLL. (See the AUXILIARY OUTPUT section below for how to select LDETB.)

The LDETB signal will be low after self-tuning has completed but will rise when either the IF or RF PLL

nears the limit of its compensation range (LDETB will also be high when either PLL is executing the self-tuning algorithm). The output frequency will still be locked when LDETB goes high, but the PLL will eventually lose lock if the temperature continues to drift in the same direction. Therefore, if LDETB goes high both the IF and RF PLLs should promptly be re-tuned by initiating the self-tuning algorithm.

Output Frequencies

The IF and RF output frequencies are set by programming the N Divider registers. Each RF PLL has its own N register and can be programmed independently. All three PLL R dividers are fixed at R=65 to yield a 200 kHz phase detector update rate from a 13 MHz reference frequency. Programming the N divider register for either RF1 or RF2 automatically selects the associated output.

The reference frequency on the XIN pin is divided by R and this signal is input to the PLL's phase detector. The other input to the phase detector is the PLL's VCO output frequency divided by N. The PLL acts to make these frequencies equal. That is, after an initial transient

$$\frac{F_{OUT}}{N} = \frac{F_{REF}}{65}$$

or

$$F_{OUT} = \frac{N}{65} \cdot F_{REF}$$

For XIN = 13 MHz this simplifies to

$$F_{OUT} = N \cdot 200\ kHz$$

The integer N is set by programming the RF1 N Divider register (register 3), the RF2 N Divider register (register 4), and the IF N Divider register (register 5).

Each N divider is implemented as a conventional high speed divider. That is, it consists of a dual-modulus prescaler, a swallow counter, and a lower speed synchronous counter. However, the calculation of these values is done automatically. Only the appropriate N value needs to be programmed

PLL Loop Dynamics

The transient response for each PLL has been optimized for a GSM application. VCO gain, phase detector gain, and loop filter characteristics are not programmable.

The settling time for each PLL is directly proportional to its phase detector update period Tϕ (Tϕ equals 1/fϕ). For a GSM application with a 13 MHz reference frequency, the RF and IF PLLs Tϕ = 5 µS. During the first 6.5 update periods, the Si4133G-X2 executes the self-tuning algorithm. Thereafter the PLL controls the output frequency. Because of the unique architecture of the Si4133G-X2 PLLs, the time required to settle the output frequency to 0.1 ppm error is approximately 21 update periods. Thus, the total time after power-up or a change in programmed frequency until the synthesized frequency is well settled (including time for self-tuning) is around 28 update periods or 140 µS.

RF and IF Outputs

The RFOUT and IFOUT pins are driven by amplifiers that buffer the RF VCOs and IF VCO, respectively. The RF output amplifier receives its input from either the RF1 or RF2 VCO, depending upon which N divider register was last written to. For example, programming the N divider register for RF1 automatically selects the RF1 VCO output.

The RFOUT pin must be coupled to its load through an ac coupling capacitor. A matching network is required to maximize power delivered into a 50 Ω load. The network consists of a 2 nH series inductance, which may be realized with a PC board trace, connected between the RFOUT pin and the ac coupling capacitor.

The network is made to provide an adequate match to an external 50 Ω load for both the RF1 and RF2 frequency bands. The matching network also filters the output signal to reduce harmonic distortion. A 50 Ω load is not required for proper operation of the Si4133G-X2. Depending on transceiver requirements, the matching network may not be needed. See Figure 16 below.

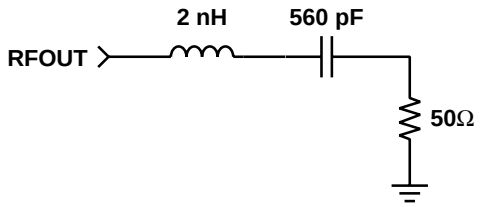


Figure 16. RFOUT 50Ω Test Circuit

The RF output power is controlled with the RFPWR bit in register 0. Setting this bit increases the supply current by approximately 1.2 mA. To minimize output power variation over temperature, the RFPWR bit can be set as a function of temperature. For example, set RFPWR=1 for temperatures greater than 50°C, otherwise set RFPWR=0.

The IFOUT pin must also be coupled to its load through an ac coupling capacitor. A matching network is also required in order to drive a 50 Ω load. See Figure 17 below.

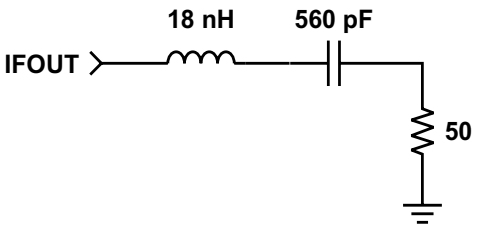


Figure 17. IFOUT 50Ω Matching Network

Reference Frequency Amplifier

The Si4133G-X2 provides a reference frequency amplifier. If the driving signal has CMOS levels it can be connected directly to the XIN pin. Otherwise, the reference frequency signal should be ac coupled to the XIN pin through a 100 pF capacitor.

Power Down Modes

Table 8 summarizes the power down functionality. The Si4133G-X2 can be powered down by taking the PWDNB pin low or by setting bits in the Power Down register (register 2). When the PWDNB pin is low, the Si4133G-X2 will be powered down regardless of the Power Down register settings. When the PWDNB pin is high, power management is under control of the Power Down register bits.

It may be desirable to defeat power down of the reference frequency amplifier. In such a case the XPDM (XTAL Power Down Mode) bit in the Main Configuration register (register 0) should be set to 1. The reference frequency amplifier will then remain powered up even when the PWDNB pin is asserted (i.e., low), excepting when all three of the Power Down register bits (PDAB, PDIB, and PDRB) are low. This exception exists so that, even in this mode, the reference amplifier can be forced to power down if sufficient time occurs for a power down and power up sequence. Alternatively, the reference amplifier power down defeat mode can be exited by setting XPDM to 0.

With the PWDNB pin high, the XPDM bit has no effect. The reference frequency amplifier, IF, and RF sections of the Si4133G-X2 circuitry can be individually powered down by setting the Power Down register bits PDAB, PDIB, and PDRB low, respectively. Note that the reference frequency amplifier will also be powered up if either the PDRB and PDIB bits are high, even if the PDAB bit is low. Also, setting the AUTOPDB bit to 1 in the Main Configuration register (register 0) is equivalent to setting all three of the bits in the Power Down register to 1. The serial interface remains available and can be written in all power down modes.

Auxiliary Output (AUXOUT)

The AUXOUT pin can be used to monitor a variety of signals. The signal appearing on AUXOUT is selected by setting the AUXSEL bits in the Main Configuration register (register 0). The possible outputs are listed in the description of the Main Configuration register.

Some of these signals may only be useful for evaluation purposes (in particular, the PLL R-divider and N-divider outputs). Two signals, have more general use. The first is the LDETB signal, which can be selected by setting the AUXSEL bits to 011. As discussed previously, this signal can be used to indicate that the IF or RF PLL is about to lose lock due to excessive ambient temperature drift and should be re-tuned. The second is the Reference Clock output. This is a buffered version of the signal on the XIN pin, with the exception that it will be held low when the reference frequency amplifier is powered down.

Table 8. Power Down Configuration

PWDNB Pin	AUTOPDB	PDIB	PDRB	Reference Frequency Amplifier	IF Circuitry	RF Circuitry
PWDNB = 0	X	X	X	OFF	OFF	OFF
PWDNB = 1	0	0	0	OFF	OFF	OFF
	0	0	1	ON	OFF	ON
	0	1	0	ON	ON	OFF
	0	1	1	ON	ON	ON
	0	0	0	ON	OFF	OFF
	1	x	x	ON	ON	ON
Note: The XPDM bit has no effect when the PWDNB pin is high.						

Control Registers

Table 9. Register Summary

Register	Name	Bit 17	Bit 16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Main Configuration	X	X	X	AUXSEL			0	0	0	0	0	0	0	0	AUTO PDB	0	1	0
1	Reserved																		
2	Power Down	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	PDIB	PDRB
3	RF1 N Divider	N_{RF1}																	
4	RF2 N Divider	X	N_{RF2}																
5	IF N Divider	X	X	N_{IF}															
6	Reserved																		
7	Reserved																		
. . .																			
15	Reserved																		

Note: X = Don't Care. Registers 1 and 6–15 are reserved. Writes to these registers may result in unpredictable behavior. Any register not listed here is reserved and should not be written.

Register 0. Main Configuration Address Field = A[3:0] = 0000

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	X	X	X	AUXSEL			0	0	0	0	0	0	0	0	AUTO PDB	0	1	0

Bit	Name	Function
17:15	Reserved	Don't care.
14:12	AUXSEL	**Auxiliary Output Pin Definition.** 000 = Reserved. 001 = Force output low. 010 = CMOS level of f_{REF}. 011 = Lock Detect—LDETB. 100 = CMOS level of $f_{\phi R}$ of active RF synthesizer. 101 = CMOS level of $f_{\phi R}$ of IF synthesizer. 110 = CMOS level of $f_{\phi N}$ of active RF synthesizer. 111 = CMOS level of $f_{\phi N}$ of IF synthesizer.
11:5	Reserved	Program to zero.
4	Reserved	Program to zero.
3	AUTOPDB	**Auto Power Down** 0 = Software powerdown is controlled by register 2. 1 = Equivalent to setting all bits in register 2 = 1.
2	Reserved	Program to zero.
1	Reserved	Program to one.
0	Reserved	Program to zero.

Register 2. Power Down Address Field (A[3:0]) = 0010

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	PDIB	PDRB

Bit	Name	Function
17:2	Reserved	Don't care.
1	PDIB	**Power Down IF Synthesizer.** 0 = IF synthesizer powered down. 1 = IF synthesizer on.
0	PDRB	**Power Down RF Synthesizer.** 0 = RF synthesizer powered down. 1 = RF synthesizer on.

Register 3. RF1 N Divider Address Field (A[3:0]) = 0011

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	N_{RF1}																	

Bit	Name	Function
17:0	N_{RF1}	**N Divider for RF1 Synthesizer.**

Register 4. RF2 N Divider Address Field = A[3:0] = 0100

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	X	N_{RF2}																

Bit	Name	Function
17	Reserved	Don't care.
16:0	N_{RF2}	**N Divider for RF2 Synthesizer.**

Register 5. IF N Divider Address Field (A[3:0]) = 0101

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	X	X	N_{IF}															

	Name	Function
17:16	Reserved	Don't care.
15:0	N_{IF}	**N Divider for IF Synthesizer.** Only the following values are allowed (frequencies assume XIN is 13 MHz): 7150 = 1070.4 MHz 7215 = 1080.0 MHz 7280 = 1089.6 MHz

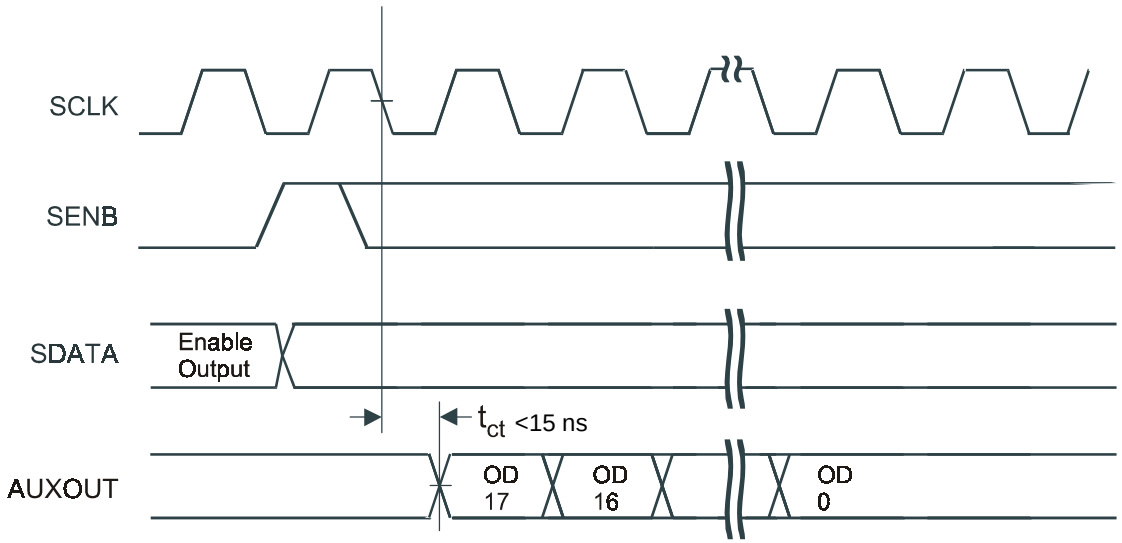
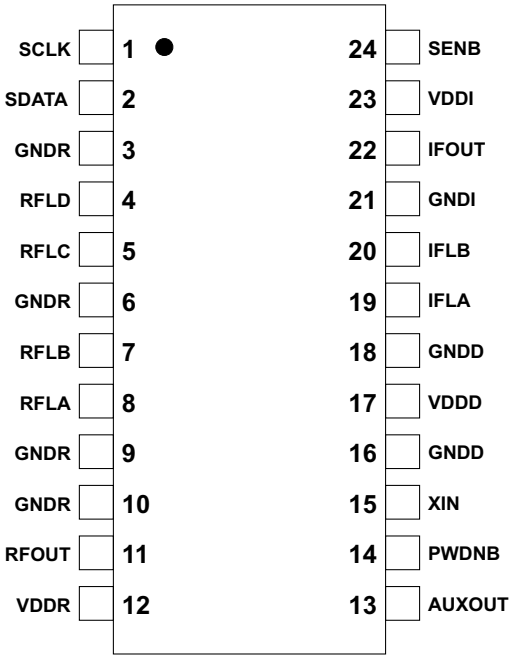


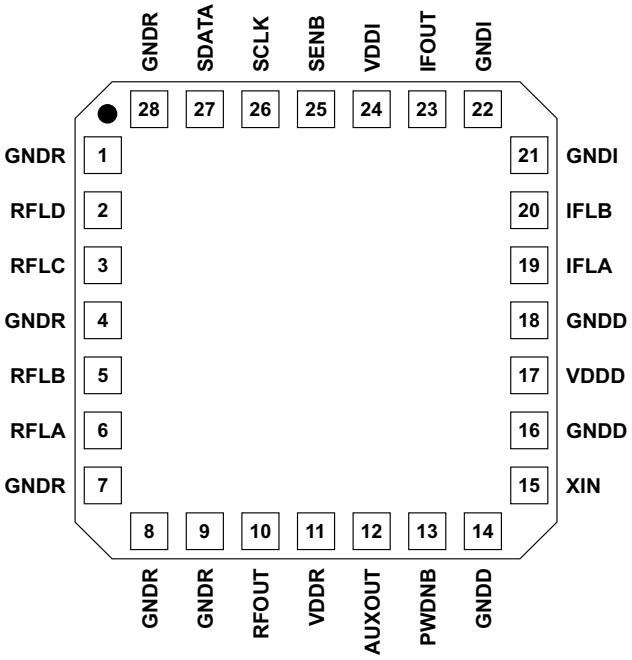
Figure 18. AUXOUT Timing Diagram

Pin Descriptions: Si4133G-XT2



Name	Pin Number(s)	Description
AUXOUT	13	Auxiliary output
GNDD	16, 18	Common ground for digital circuitry
GNDI	21	Common ground for IF analog circuitry
GNDR	3, 6, 9, 10	Common ground for RF analog circuitry
IFLA, IFLB	19, 20	Pins for inductor connection to IF VCO
IFOUT	22	Intermediate frequency (IF) output of the IF VCO
PWDNB	14	Power down input pin
RFLA, RFLB	7, 8	Pins for inductor connection to RF1 VCO
RFLC, RFLD	4, 5	Pins for inductor connection to RF2 VCO
RFOUT	11	Radio frequency (RF) output of the selected RF VCO
SCLK	1	Serial clock input
SDATA	2	Serial data input
SENB	24	Enable serial port input
VDDD	17	Supply voltage for digital circuitry
VDDI	23	Supply voltage for IF analog circuitry
VDDR	12	Supply voltage for the RF analog circuitry
XIN	15	Reference frequency amplifier input

Pin Descriptions: Si4133G-XM2



Name	Pin Number(s)	Description
AUXOUT	12	Auxiliary output
GNDD	14, 16, 18	Common ground for digital circuitry
GNDI	21, 22	Common ground for IF analog circuitry
GNDR	1, 4, 7-9, 28	Common ground for RF analog circuitry
IFLA, IFLB	19, 20	Pins for inductor connection to IF VCO
IFOUT	23	Intermediate frequency (IF) output of the IF VCO
PWDNB	13	Power down input pin
RFLA, RFLB	5,6	Pins for inductor connection to RF1 VCO
RFLC, RFLD	2, 3	Pins for inductor connection to RF2 VCO
RFOUT	10	Radio frequency (RF) output of the selected RF VCO
SCLK	26	Serial clock input
SDATA	27	Serial data input
SENB	25	Enable serial port input
VDDD	17	Supply voltage for digital circuitry
VDDI	24	Supply voltage for IF analog circuitry
VDDR	11	Supply voltage for the RF analog circuitry
XIN	15	Reference frequency amplifier input

Ordering Guide

Ordering Part Number	Description	Package	Temperature
Si4133G-XM2	RF1 / RF2 / IF OUT	28-Pin MLP	–20 to 85°C
Si4133G-XT2	RF1 / RF2 / IF OUT	24-Pin TSSOP	–20 to 85°C

Package Outline: Si4133G-XT2

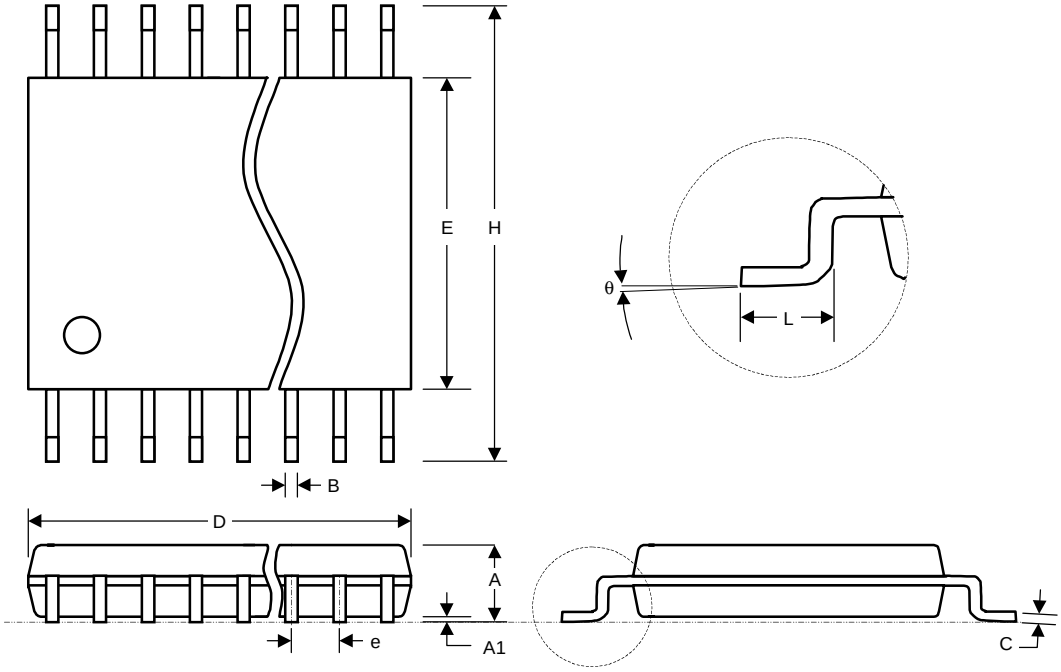


Figure 19. 24-Pin Thin Shrink Small Outline Package (TSSOP)

Table 10. Package Dimensions

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	—	0.047	—	1.1
A1	0.002	0.006	0.05	0.15
B	0.007	0.012	0.19	0.30
C	0.004	0.008	0.09	0.20
D	0.303	0.311	7.70	7.90
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.018	0.030	0.45	0.75
θ	0°	8°	0°	8°

Package Outline: Si4133G-XM2

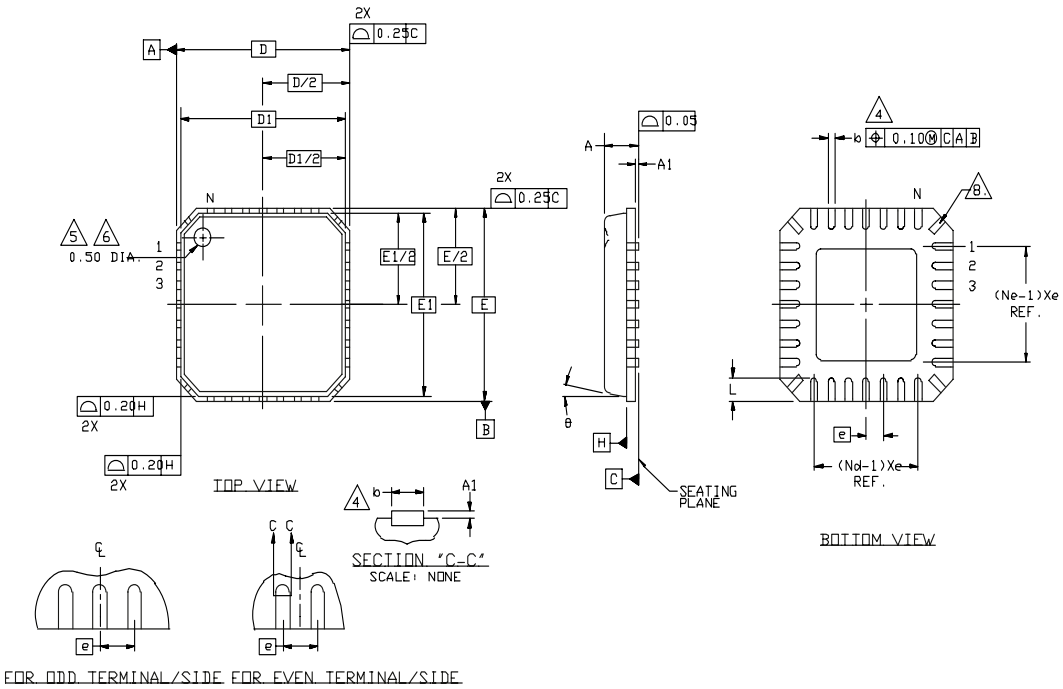


Figure 20. 28-Pin Micro Leadframe Package (MLP)

Table 11. Package Dimensions

Controlling Dimension: mm

Symbol	Millimeters		
	Min	Nom	Max
A	—	0.90	1.00
A1	0.00	0.01	0.05
b	0.18	0.23	0.30
D	5.00 BSC		
D1	4.75 BSC		
E	5.00 BSC		
E1	4.75 BSC		
N	28		
Nd	7		
Ne	7		
e	0.50 BSC		
L	0.50	0.60	0.75
θ			12°

NOTES:

NOTES:

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